WHAT IS CLAIMED IS:

1. A method for reducing memory latency during read requests, comprising:

issuing a single read request for data from a first one of a plurality of processors on a local bus;

forwarding the single read request to a memory directory associated with a home memory for the data, the home memory being either remote from or associated with the plurality of processors on the local bus according to a location of the data;

determining whether the data is located at another one of the plurality of processors on the local bus;

determining whether the data has been modified;

providing the data to the first one of the plurality of processors according to the single read request in response to whether or not the data is located in another one of the plurality of processors on the local bus and the data is modified.

2. The method of Claim 1, further comprising:

processing the single read request at the memory directory;

transferring a read response according to processing of the single read request.

3. The method of Claim 2, further comprising:

providing the read response to the first one of the plurality of processors in response to the data not being found on any of the plurality of processors or if the data has not been modified.

4. The method of Claim 2, further comprising:

discarding the single read request in response to the data being provided by another one of the plurality of processors so that it is not transferred to the first one of the plurality of processors.

5. The method of Claim 2, further comprising:

determining whether a remote processor has the data in a modified form;

obtaining the data from the remote processor in response to it having the data in a modified form;

providing the modified data in the read response.

6. The method of Claim 1, further comprising:

processing the single read request at the memory directory;

transferring a read response according to processing of the single read request prior to determining whether the data is located at another one of the plurality of processors on the local bus and determining whether the data has been modified;

waiting for the determination of whether the data is located at another one of the plurality of processors on the local bus and that the data has been modified.

7. The method of Claim 6, further comprising:

providing the read response to the first one of the plurality of processors in response to the data not being found on any of the plurality of processors or if the data has not been modified.

8. The method of Claim 1, further comprising:

initiating an update to memory request in response to receiving the data at the first one of the plurality of processors, the update to memory request indicating that a read request is outstanding.

9. The method of Claim 8, further comprising:

receiving the update to memory request at the memory directory prior to receipt of the read request.

10. The method of Claim 9, further comprising:

ignoring the single read request pursuant to the update to memory request.

11. A system for reducing memory latency during read requests, comprising:

a plurality of processors on a local bus, a first one of the plurality of processors operable to issue a single read request for data;

a processor interface operable to receive the single read request, the processor interface operable to route the single read request to a home location for the data, the home location for the data being either remote from or associated with the plurality of processors on the local bus, the processor interface operable to determine whether the data is located in another one of the plurality of processors and whether it has been modified, the processor interface operable to provide the data to the first one of the plurality of processors in response to the single read request whether or not the data is available locally and is modified.

12. The system of Claim 11, further comprising:

a memory directory associated with a home location of the data, the memory directory operable to process the single read request.

13. The system of Claim 12, wherein the memory directory generates a read response according to the single read request for transfer to the processor interface.

14. The system of Claim 13, wherein the processor interface receives the read response, the processor interface operable to determine whether the data has been locally provided to the first one of the plurality of processors, the processor interface operable to discard the read response in accordance with the data being locally provided.

15. The system of Claim 13, wherein the processor interface receives the read response, the processor interface operable to determine whether the data has been locally provided to the first one of the plurality of processors, the processor interface operable to provide the read response to the first one of the plurality of processors in accordance with the data not being locally provided.

16. The system of Claim 11, wherein the first one of the plurality of processors is operable to generate an update to memory request in response to locally receiving the data, the update to memory request including an indication that the single read request is outstanding.

17. The system of Claim 16, wherein the memory directory receives the update to memory request prior to the read request.

18. The system of Claim 16, wherein the memory directory is operable to ignore the read request in response to the indication in the update to memory request.

19. A system for reducing memory latency during read requests, comprising:

means for issuing a single read request for data from a first one of a plurality of processors on a local bus;

means for forwarding the single read request to a memory directory associated with a home memory for the data, the home memory being either remote from or associated with the plurality of processors on the local bus according to a location of the data;

means for determining whether the data is located at another one of the plurality of processors on the local bus;

means for determining whether the data has been modified;

means for providing the data to the first one of the plurality of processors according to the single read request in response to whether or not the data is located in another one of the plurality of processors on the local bus and the data is modified.

20. The system of Claim 19, further comprising:

means for initiating an update to memory request in response to receiving the data at the first one of the plurality of processors, the update to memory request indicating that a read request is outstanding; and

means for receiving the update to memory request at the memory directory prior to receipt of the read request.